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7590	08/09/2004		EXAMINER	
DAVID L MCCOMBS			BUTLER, DENNIS	
HAYNES AN BOONE LLP			ART UNIT	PAPER NUMBER
901 MAIN STREET			2115	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	09/707,585	Applicant(s)	VERDUN, GARY J.
Examiner	Dennis M. Butler	Art Unit	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 May 2004.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-6, 11, 14 and 15 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-6, 11, 14 and 15 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. _____.
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____. 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

1. This action is in response to amendment B received on May 21, 2004.

Claims 1-6, 11 and 14-15 are pending.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-6, 11 and 14-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification fails to describe a south bridge controller performing power state transitions from the I/O devices to the south bridge controller as recited in claims 1 and 11. The examiner could not find a description of the above element, that was added in amendment B, in the specification. In addition, applicant has not pointed out where the claim limitation of a south bridge controller performing power state transitions from the I/O devices to the south bridge controller is supported in the specification. See MPEP 706.03(o) and 2163.06.

5. Claims 1-6, 11 and 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 11, the phrase "a south bridge controller ... performing power state transitions from the I/O devices to the south bridge controller" is unclear as to its meaning. The phrase is unclear as to its relationship to asserting a transition to a different operating mode on the processor and the processor having various power state conditions.

Claims 2-6 and 14-15 are rejected because they incorporate the deficiencies of claim 1 and 11.

6. Claims 1-2 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole, II, U. S. Patent 6,496,888.

Per claim 1:

A) Pole, II teaches the following claimed items:

1. a processor with various power state conditions that performs at a selectable operating mode with processor 202 of figure 2 and at column 2, line 61 – column 3, line 25;

2. a north bridge controller initiating a processor reset signal input with chipset logic 214 of figure 2, at column 4, lines 15-26, with figures 3 and 4B and at column 5, lines 15-17 and 50-65;

3. a south bridge controller providing an interface for I/O devices and performing power state transitions with bus bridge 226 of figure 2, at column 4, lines 32-45 and at column 5, lines 3-4 and 27-33;

4. a clock at column 4, lines 46-55 and at column 5, lines 40-49;
5. a power supply with the AC power supply corresponding to the AC power source and/or the battery at column 2, line 61 – column 3, line 10;
6. a logic device interfaces to the above elements that asserts a transition to a different operating mode on the processor while the processor is in a deep sleep state with the chip set logic and the bus ratio strap option logic of figures 2 and 3, with figure 4B, at column 3, lines 11-25, at column 5, line 11-39 and at column 6, line 41 – column 7, line 4;
7. the clock providing a frequency and the power supply providing a voltage matched to the different operating mode upon transition at column 2, line 61 – column 3, line 10.

Regarding the north bridge controller initiating a processor reset signal input, Pole, II describes that the bus ratio register is incorporated into a chip set component that generates control signals during a processor reset. Pole, II shows that the bus ratio register is located in the north bridge (chip logic 214) with figures 2 and 3 and shows that a processor reset signal is generated during a processor reset sequence with figure 4B. Therefore, the north bridge is described as generating a processor reset signal input.

Per claims 2, 5 and 6:

Pole describes the logic device monitoring a reset condition of the processor, waiting for the reset to be deasserted and asserting a performance mode transition with figure 4B and at column 6, line 60 –

column 7, line 4. Pole describes asserting either the high performance mode or the low performance mode during normal processor power up sequence (system power up) that includes accessing a ROM (loading system settings from ROM) at column 5, line 67 – column 6, line 10.

7. Claims 3-4, 11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pole, II, U. S. Patent 6,496,888 in view of Pole, II et al., U. S. Patent 6,272,642.

Per claims 3-4, and 11:

A) Pole, II teaches the following claimed items:

1. a processor with various power state conditions that performs at a selectable operating mode with processor 202 of figure 2 and at column 2, line 61 – column 3, line 25;
2. a north bridge controller initiating a processor reset signal input with chipset logic 214 of figure 2, at column 4, lines 15-26, with figures 3 and 4B and at column 5, lines 15-17 and 50-65;
3. a south bridge controller providing an interface for I/O devices and performing power state transitions with bus bridge 226 of figure 2, at column 4, lines 32-45 and at column 5, lines 3-4 and 27-33;
4. transitioning the processor into a different operating mode with figures 2, 3 and 4B, at column 3, lines 11-25, at column 5, line 11-39 and at column 6, line 41 – column 7, line 4;

5. waiting for the processor to reach a reset state, resetting the processor and asserting a performance mode change in the processor with figure 4B and at column 6, line 41 – column 7, line 4.

Regarding the north bridge controller initiating a processor reset signal input, Pole, II describes that the bus ratio register is incorporated into a chip set component that generates control signals during a processor reset. Pole, II shows that the bus ratio register is located in the north bridge (chip logic 214) with figures 2 and 3 and shows that a processor reset signal is generated during a processor reset sequence with figure 4B. Therefore, the north bridge is described as generating a processor reset signal input.

B) The claims seem to differ from Pole, II in that Pole, II fails to explicitly teach passing control signals from a north bridge or south bridge controller capable of placing the processor in a deep sleep state as claimed.

C) However, Pole, II describes that the chip set logic is divided into a North Bridge and a South Bridge and that the logic could be included in the North or South Bridge or in a single chip that integrates both bridges at column 4, line 64 – column 5, line 39. Pole, II further describes placing the bus ratio register that sets the operating mode of the processor into the chipset component that generates control signals during a processor reset sequence at column 5, lines 11-17. Pole, II describes placing the processor in a deep sleep state and transitioning it to a different operating

mode with figure 4b. Pole, II suggests that the chip set/bridge passes control signals capable of placing the processor in a deep sleep state using system control logic and system management bus interface of the chip set at column 5, lines 19-21, at column 7, lines 50-55 and at column 8, lines 24-46. However, Pole, II does not explicitly recite that control signals capable of placing the processor in a deep sleep state are passed from the chip set or bridge. Pole, II et al teach that it is known to include a bridge that passes control signals capable of placing the processor in a deep sleep state with figures 1, 2 and 4, at column 3, line 66 – column 4, line 30 and at column 4, lines 55-61. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a north or a south bridge that passes control signals capable of placing the processor in a deep sleep state, as suggested by Pole, II in view of Pole, II et al, in order to incorporate the bus ratio register into a chip set that generates control signals during the deep sleep and reset sequence for transitioning the processor into a different operating mode. One of ordinary skill in the art would have been motivated to combine Pole, II and Pole, II et al because of Pole, II suggestion of incorporating the bus ratio register into a chip set (north and/or south bridge) that generates control signals during the reset sequence at column 5, lines 15-26, with figure 4b and at column 6, lines 41-67 and because of Pole, II et al's suggestion of integrating power management control logic into a host and a system bridge at column 4, lines 2-8. It would have been obvious for

one of ordinary skill in the art to combine Pole, II and Pole, II et al because they are both directed to the problem of placing a processor into a deep sleep state and transitioning the processor into a different operating/performance mode.

Per claims 14 and 15:

Pole, II describes asserting either the high performance mode or the low performance mode during normal processor power up sequence (system power up) that includes accessing a ROM (loading system settings from ROM) at column 5, line 67 – column 6, line 10. Since Pole describes selecting either a high or low performance mode during system boot, the system clearly can be set to assert the high performance mode during normal processor power up sequence (system power up).

8. Applicant's arguments filed on May 21, 2004 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. the Pole, II reference is defective, does not teach any of the recited

elements of claim 1 and the examiner has not produced a *prima facie* case.

B. There is no basis for combining the references because neither Pole II nor Pole II, et al teach or even suggests the desirability of the combination.

C. The examiner's combination arises solely from hindsight.

9. As to point A, the examiner disagrees with applicant's contentions. Pole, II teaches all of the claimed elements and the examiner has pointed out in detail including the figures, column numbers and the line numbers of the corresponding sections showing each claim limitation. Therefore, the examiner has produced a *prima facie* case and the burden now shifts to applicant. In the response, applicant has copied claim 1 in its entirety and contends that Pole, II teaches none of the claimed elements. However, it is believed that any one of ordinary skill in the power control art would clearly acknowledge that Pole, II describes the processor with various power state conditions, the north bridge, the south bridge, the clock, the power supply and logic that performs the recited functions. It is unclear why applicant amended claim 1 if Pole, II reference did not teach any of the claimed elements. Applicant's copying of claim 1 as the basis of their argument amounts to an unfounded allegation and does not comply with the rules of practice. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. In addition, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The examiner has produced a *prima facie* case, the

Pole, II is not defective and it teaches each of the claimed elements as described in the above rejection.

As to point B, the examiner disagrees with applicant's contentions. The examiner has provided clear motivation for combining Pole, II and Pole, II et al in the above rejection. Pole, II describes that the processor must be put into a deep power down or sleep mode when performing a bus ratio change sequence with figure 4B and at column 6, lines 41-55. Pole, II describes that a bridge chipset component generates control signals during a processor reset sequence at column 5, lines 15-26. As described in the rejection, Pole, II clearly suggests that the bridge chipset logic that performs the reset sequence also places the processor into the deep sleep mode because this step is included in the processor reset sequence performed by the chipset, column 6, lines 24-25. Pole, II et al teach that it is known to include a bridge chipset that passes control signals capable of placing the processor in a deep sleep state with figures 1, 2 and 4, at column 3, line 66 – column 4, line 30 and at column 4, lines 55-61. In addition, Pole, II and Pole, II et al are both directed to the problem of placing a processor into a deep sleep state and transitioning the processor into a different operating/performance mode. Furthermore, both references use the same chipset, the Intel North Bridge and south bridge chipset. Both references are assigned to Intel and both references include the common inventor Edwin J. Pole, II. The examiner contends that the north south chipset of Pole, II generates deep sleep control signals that place the processor in the deep sleep state because it has the same power control capabilities as the north south chipset

of Pole, II et al. The circuit court has rejected the notion that an express written motivation to combine must appear in prior art references and has found motivation to combine references based on the nature of the problem to be solved and because the references were directed to precisely the same problem.

Ruiz v. A.B. Chance Co., 357 F.3d 1270, 69 USPQ2d 1686 (Fed. Cir. 2004). In addition, the court has found that the normal desire of scientists or artisans to improve upon what is already generally known provides the motivation to determine where in a disclosed set of percentage ranges is the optimum combination of percentages. *In re Peterson* 01/08/2003.

As to point C, in response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Dennis M. Butler
Primary Examiner
Art Unit 2115